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Help

Logout

Interrupt

Main Menu

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Edit S Numbers

Preferences

Cases

Search Results -

Terms	Documents
L8 and (register with (point adj2 point))	0

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Set Name Query

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<u>L10</u>	L8 and (register with (point adj2 point))	0	<u>L10</u>
<u>L9</u>	L8 and ((ring with bus) same module)	0	<u>L9</u>
<u>L8</u>	L7 same l6	79	<u>L8</u>
<u>L7</u>	bus near8 (width or bandwidth or size or wide or capacity)	5732	<u>L7</u>
<u>L6</u>	(module or DIMM or SIMM or card) near8 (data near4 bus)	1940	<u>L6</u>

DB=USPT; PLUR=YES; OP=ADJ

<u>L5</u>	l3 and (register with (point adj2 point))	0	<u>L5</u>
<u>L4</u>	l3 and ((ring with bus) same module)	18	<u>L4</u>
<u>L3</u>	L2 same l1	445	<u>L3</u>
<u>L2</u>	bus near8 (width or bandwidth or size or wide or capacity)	19570	<u>L2</u>
<u>L1</u>	(module or DIMM or SIMM or card) near8 (data near4 bus)	6054	<u>L1</u>

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99%

J. D. Nicoud , K. Skala

ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture June 1986

Volume 14 Issue 2

In order to build lower cost multimicroprocessor systems, a narrow synchronous bus (15 active lines) is proposed. It multiplexes address and data on 8 bits, and arbitrates in two pipe-lined cycles on four lines. Due to the 20 to 40 MHz bus clock, and the pipelined control logic, the performances are equivalent to Multibus-2, IEEE-P896 and similar 32-bit buses. For the implementation, cards are disposed radially around a special connector. The very short co ...

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- ☐ Standards

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- ☐ Advanced

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- ☐ Conference Proceedings
- ☐ Standards

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- ☐ Basic
- ☐ Advanced

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